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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/691,353 | 10/18/2000 | James W. Adkisson | BUR9-1999-0300-US1 | 3972 |

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| EXAMINER | |
|---|---|
| NGUYEN, KHIEM D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2823 | |

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/691,353 | ADKISSON ET AL. | |
| | Examiner | Art Unit | |
| | Khiem D Nguyen | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 14-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 14-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *New Grounds of Rejection*

### *Claim Rejections - 35 USC § 102*

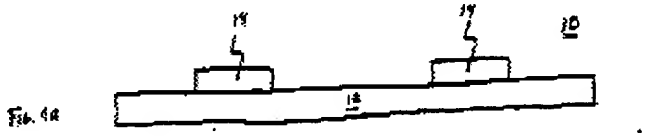
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

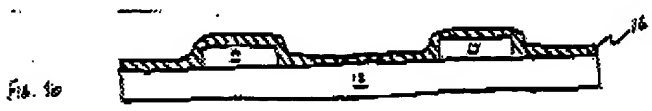
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 14-19 and 22-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Doyle (U.S. Pub. 2003/0006410).

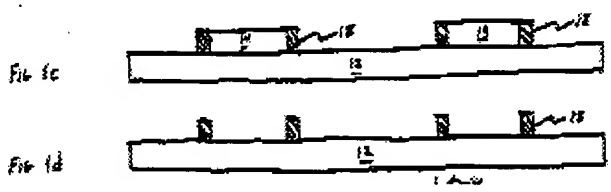
In re claim 1, **Doyle** discloses a method of forming a field effect transistor (FET) transistor, comprising: providing a substrate **12**; forming a layer **14** on the substrate, the layer having exposed vertical side surfaces on opposite sides of the layer (page 2, paragraph [0034] and **FIG. 1a**);



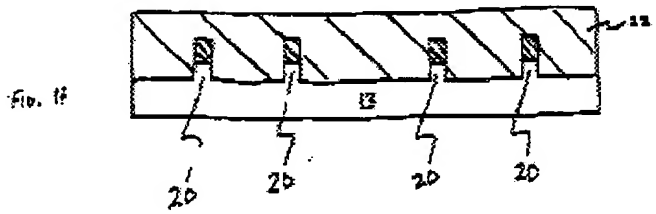
forming an epitaxial channel **16** on the each of the exposed side surfaces of the layer, the channel having an exposed first sidewall opposite the vertical side surface of the layer (page 2, paragraph [0034] and **FIG. 1b**);

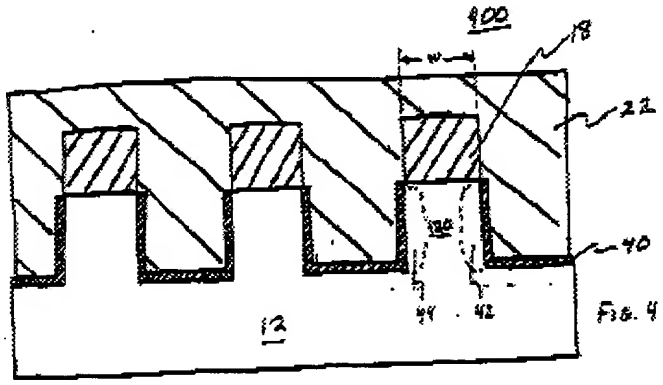


removing a channel on a first vertical side surface of the layer (page 2, paragraphs [0036]-[0037] and **FIG. 1c**) and then removing the layer (page 2, paragraph [0037] and **FIG. 1d**), thereby exposing a second vertical sidewall of the channel formed on the second vertical side of the layer;



forming a second channel **20** in place of removed channel; and forming a gate **22** adjacent to at least one of the sidewalls of the channel and the second channel (**42** and **44**), there being a gate dielectric **40** between each channel (**42** and **44**) and the gate **22** (page 2, paragraph [0039], page 3, paragraph [0051] and **FIGS. 1f** and **4**).





In re claim 14, **Doyle** discloses a method for forming a double gated field effect transistor (FET), comprising the steps of: forming on a substrate a first and second

epitaxially grown channels, the channels having vertical side surfaces extending up from the substrate, wherein the second channel is grown following removal of a central semiconductor region centered between the channels upon one of whose opposite vertical sides the first channel was grown (page 2, paragraphs [0036]-[0037] and **FIGS. 1c-d**); etching areas within a silicon layer to form a source and a drain, wherein a side surfaces of the source and the drain contact opposing end surfaces of the first and second epitaxially grown channels; and forming a gate **22** that contacts a top surface and two side surfaces of the first and second epitaxially grown channels (**42** and **44**) and a top surface of the substrate **12** (page 2, paragraph [0039], page 3, paragraph [0051] and **FIGS. 1f** and **4**).

In re claim 15, **Doyle** discloses wherein the forming step comprises the steps of: forming first and second semiconductor lines **14**, each end of the silicon lines contacting one of the source and the drain (page 2, paragraph [0041] and **FIG. 2a**);

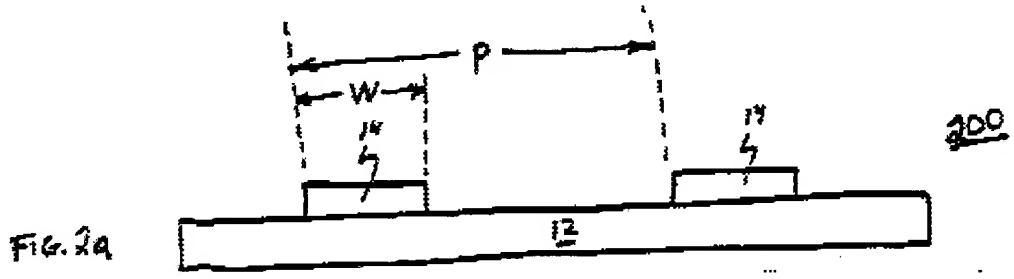


FIG. 2a

forming an etch stop layer **16** on an exposed side surface of each of the first and second semiconductor lines (page 2, paragraph [0042] and **FIG. 2b**);

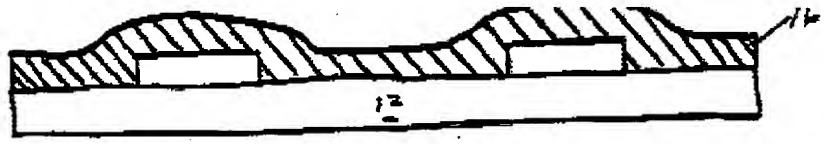
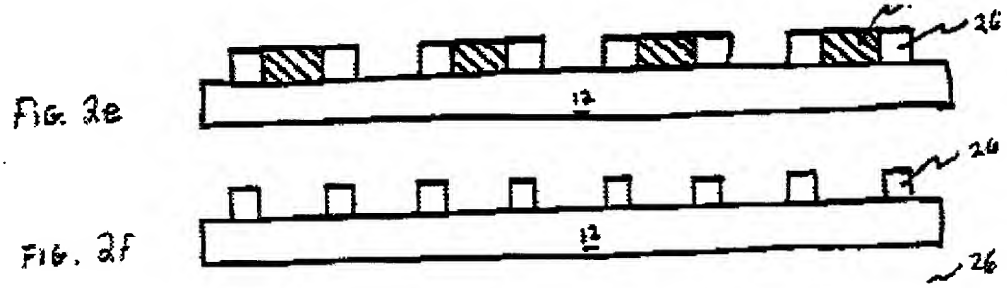


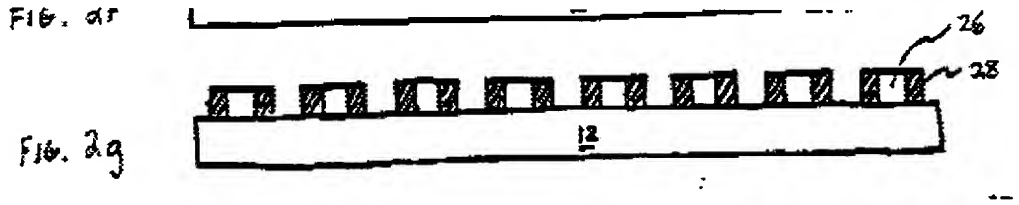
FIG. 2b

epitaxially growing first and second semiconductor layers **24** on each etch stop layer (page 2, pragraph 0043] and **FIG. 3c**);


etching away the first and second semiconductor lines **14** and the etch stop layers 16 (page 3, paragraphs [0044]-[0045] and **FIGS. 2e-f**);



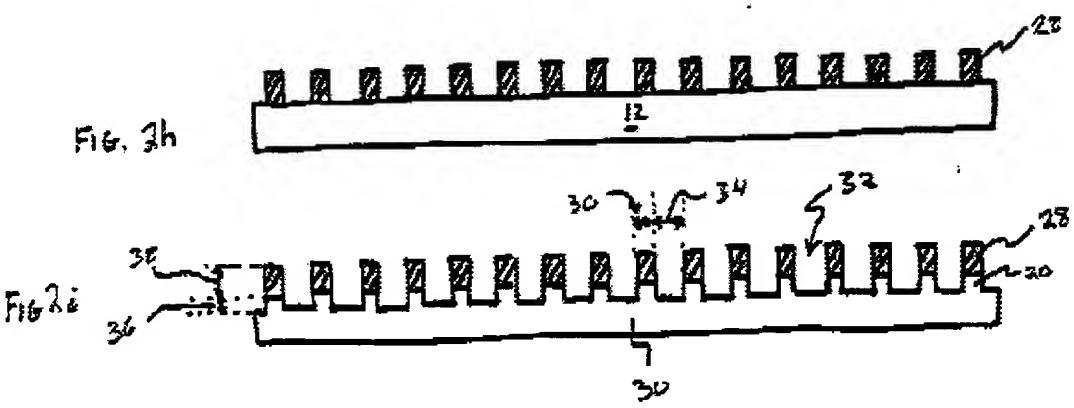

filling areas surrounding the first and second epitaxially grown semiconductor layers and between the source and the drain with an oxide fill **26** (page 3, paragraph [0046 and **FIG. 2g**);




and etching a portion of the oxide fill to form an area that defines a gate **22**, wherein the area that defines the gate is substantially centered between and substantially parallel to the source and the drain (page 3, paragraph [0051] and **FIG. 4**);

In re claim 16, **Doyle** discloses wherein the method as recited in claim 15, further comprising the steps of: etching the oxide fill between the gate the source to expose the

first and second epitaxially grown silicon layers; and etching the oxide fill between the gate and the drain to expose the first and second epitaxially grown silicon layers (page 3, paragraphs [0046]-0047] and **FIGS. 2h-i**).




In re claim 17, **Doyle** discloses wherein the method as recited in claim 16, further comprising the step of forming an oxide on the first and second epitaxially grown silicon layers **(FIG. 2d)**.

In re claim 18, **Doyle** discloses wherein the oxide is silicon dioxide (page 3, paragraph [0044]).

In re claim 19, **Doyle** discloses wherein the method as recited in claim 14, further comprising the steps of: implanting a portion of the epitaxially grown silicon layers between the gate and the source; and implanting a portion of the epitaxially grown silicon layers between the gate and the drain (page 4, paragraph [0057 and **FIG. 8**).

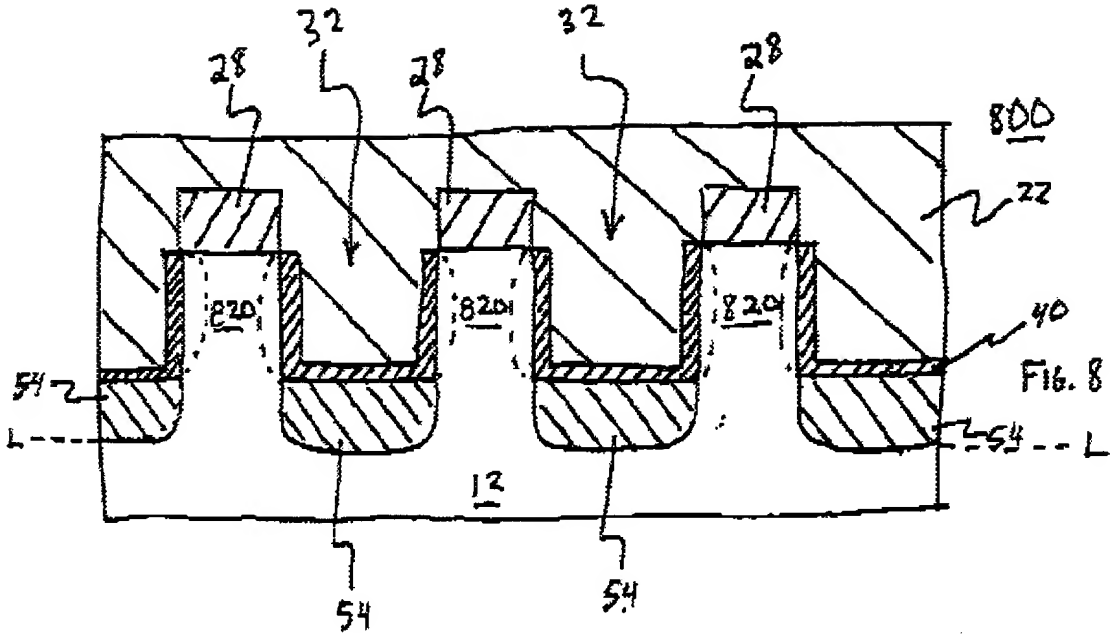



Fig. 8

In re claim 22, **Doyle** discloses wherein the method as recited in claim 14, further comprising the step of forming a contact on each of the gate, the source and the drain (page 4, paragraph [0059] and **FIG. 9**).

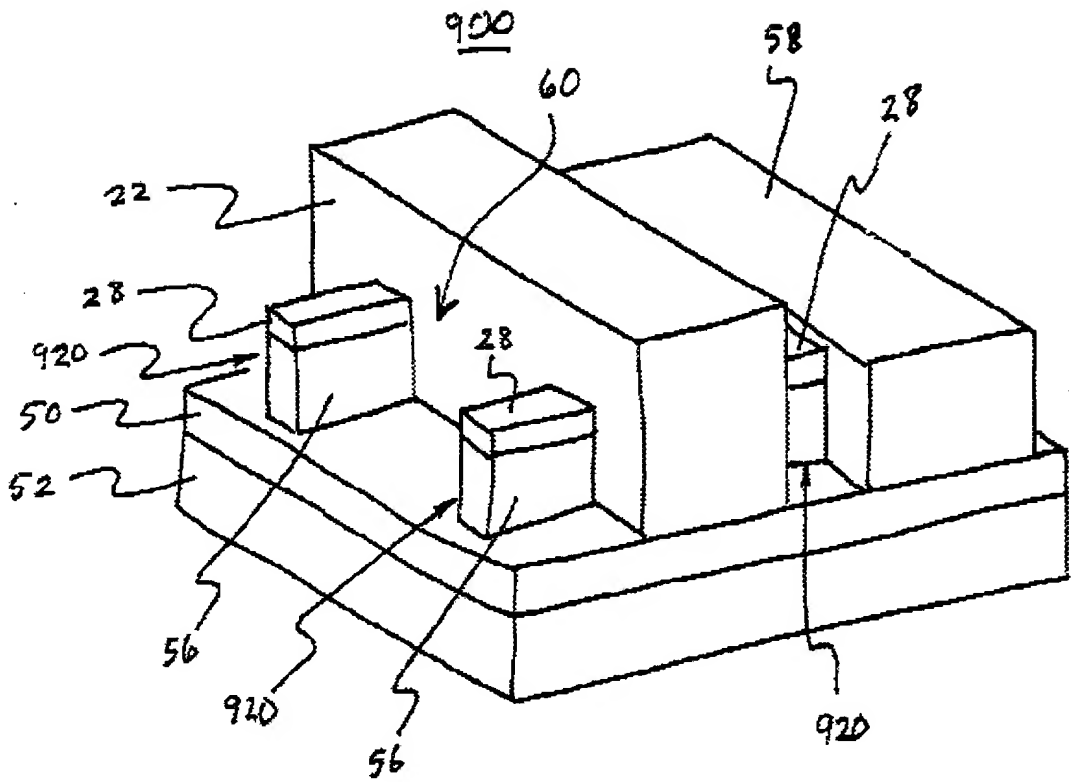



FIG. 9

In re claim 23, **Doyle** discloses wherein the method as recited in claim 14, wherein the gate material is polysilicon (page 2, paragraph [0039]).

In re claim 24, **Doyle** discloses a method of forming an FET, comprising: forming on a substrate a first semiconductor layer having first and second ends and a central region that is thinner than the first and second ends, the central region having first and second side surfaces extending upward from the substrate, epitaxially growing a semiconductor channel region on at least one of the first and second side surfaces of the central region of the first semiconductor layer, a first side of the channel being exposed; removing the central region of the first semiconductor layer, thereby exposing a second

side of the channel; forming a dielectric layer **40** on exposed surfaces of the semiconductor channel region (**42** and **44**); and forming a gate electrode **22** on the dielectric layer (page 3, paragraphs [0044]-[0051]).

In re claims 25-27, **Doyle** discloses where in the semiconductor channel region is formed of an alloy of silicon and a Group IV element wherein the semiconductor channel region is formed of a material selected from the group consisting of silicon, silicon-germanium, and silicon-germanium carbon (page 3, paragraph [0054]).

In re claim 28, **Doyle** discloses wherein the step of removing the first semiconductor layer does not appreciably remove the semiconductor channel region **(FIGS. 2a-i)**.

In re claim 29, **Doyle** discloses wherein an etch stop is epitaxially grown between the first semiconductor layer and the semiconductor channel region **(FIG. 4)**.

In re claim 30, **Doyle** discloses wherein the method as recited in claim 24, wherein the gate electrode is formed of a material selected from the group consisting of polysilicon (page 2, paragraph [0039]).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle (U.S. Pub. 2003/0006410).

In re claims 20 and 21, **Doyle** discloses implanting a portion of the epitaxially grown silicon layers between the gate and the source and implanting a portion of the epitaxially grown silicon layers between the gate and the drain (page 4, paragraph [0057 and FIG. 8) but does not explicitly disclose wherein the implanting step is in the range of 10 to 45 degrees relatives to a vector perpendicular to a top surface of the epitaxially grown silicon layers and wherein the implants are done in a series at approximately 90 degrees relative to each other.

However, there is no evidence indicating that the implanting angle ranges is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

***Response to Amendment and Arguments***

Applicant's arguments with respect to claims 1 and 14-30 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP §

706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.

W. DAVID COLEMAN
PRIMARY EXAMINER